

# A WIDEBAND pHEMT DOWNCONVERTER MMIC FOR SATELLITE COMMUNICATION SYSTEMS

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**Abstract** - This paper presents the design and performance of a broadband, low power, +3.0V pHEMT Gilbert cell downconverter IC for satellite communication systems. The downconverter is fully integrated on to a single die and requires no external matching elements. The MMIC demonstrates 300-8000 MHz RF-LO bandwidth and 185-2085 MHz IF bandwidth.

## *Introduction*

Wideband, low power, high performance downconverters are required in many satellite communication systems. In this paper the design and performance of a low power, wideband, highly integrated downconverter MMIC utilizing 0.25 $\mu$ m pHEMT technology is described. The LO-RF baluns, Gilbert cell mixer, combiner, and output driver are integrated onto a single GaAs chip. The circuit requires no external RF matching elements and is DC blocked at all RF ports. To this author's knowledge the performance of a wideband, fully integrated pHEMT Gilbert cell downconverter MMIC has not been reported. The MMIC was designed and fabricated with the TriQuint Semiconductor Texas Inc. 0.25 $\mu$ m MMW-pHEMT process.

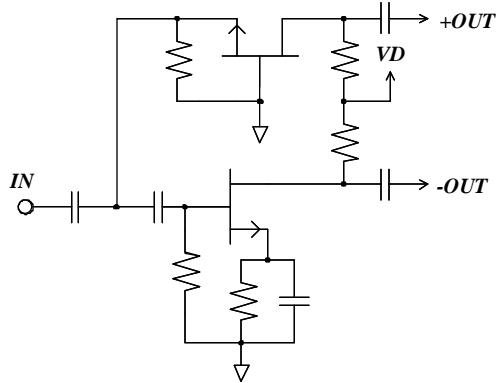
## *Circuit Design*

The performance goals for the downconverter MMIC are listed in Table 1. The requirements of low power consumption and gain flatness

over the specified bandwidth motivated the choice of 0.25 $\mu$ m pHEMT device technology for this design. The high  $f_T$  available at low DC bias conditions permits the sacrifice of excess gain such that wideband resistive matching may be employed. The circuit was designed and simulated with the LIBRA<sup>TM</sup> software package and the active devices were represented with the Materka model. The RF and LO balun circuits are the parallel connection of common source and common gate amplifiers as shown in Figure 1 [1]. The two amplifiers are biased to have the same magnitude gain, however the angle is ideally 180° out of phase. The input impedance of the common gate amplifier is approximately  $1/g_m$ , and with a properly sized device a 50 $\Omega$  impedance can be achieved.

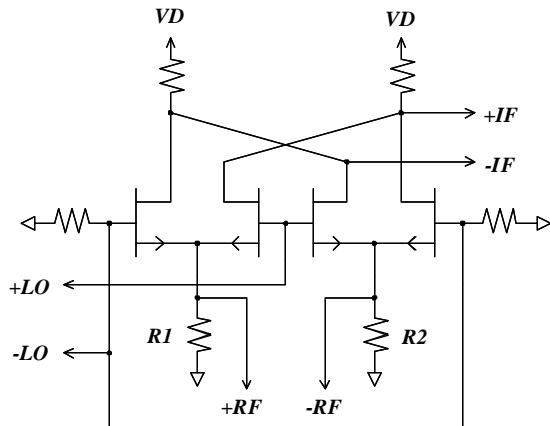
RF-LO Frequency	300 - 2500 MHz
IF Frequency	185 - 2085 MHz
Conversion Gain	> 13 dB @ IF=185 MHz
	> 8 dB @ IF=2085 MHz
Gain Variation	< 1 dB (vs. RF Freq.)
SSB Noise Figure	< 10 dB
Output TOI	> 0 dBm
LO-IF / RF Iso.	> 25 dB
LO Power	-5.0 dBm
DC Supply	+3.0 V @ < 20 mA

**Table 1. Performance goals for the down-converter MMIC.**



**Figure 1. RF / LO Balun.**

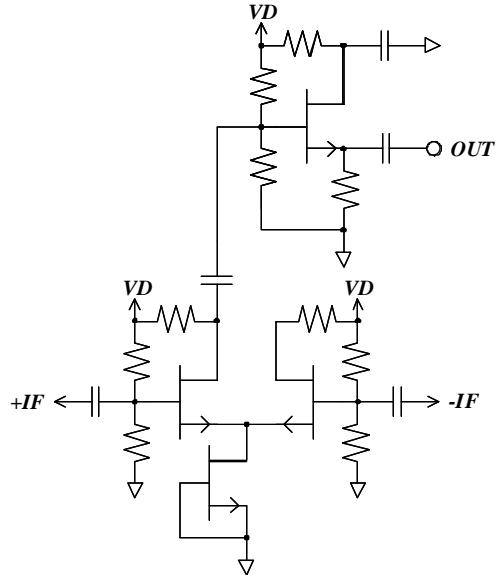
The common source circuit is designed to have a large input impedance and will not load the common gate amplifier when connected in parallel. The mixer core of the downconverter is a FET quad in a Gilbert cell arrangement as shown in Figure 2 [2].



**Figure 2. FET Gilbert Cell Mixer Core.**

The RF and LO input signals combine out of phase at the IF ports hence the circuit is a doubly balanced structure. The normal configuration has been modified for low voltage operation by replacing the RF buffer

FETs with resistors R1 and R2. These resistors also provide a self bias function and feedback to reduce the effect of device mismatch on the RF and LO isolation. The IF outputs of the mixer core are combined with the differential amplifier circuit shown in Figure 3 [3]. One arm of the differential pair drives a source follower output stage. This common drain arrangement has an output impedance approximately equal to  $1/gm$  and is sized to provide a  $50\Omega$  output impedance for the downconverter.



**Figure 3. Combiner / Output Driver.**

## Results

A photograph of the fabricated MMIC is shown in Figure 4. The die size is 2.57mm by 1.80mm, and the circuit may be RF-probed. Devices were mounted to carrier plates and the I/O ports are connected to  $50\Omega$  transmission lines with bond wires. The transmission line interface is accomplished with SMA connector launchers. The only external component used

for the testing was a 100 pF chip capacitor to bypass the DC supply voltage. The power consumption for the MMIC is 51 mW at +3.0 V. The LO drive power is -5.0 dBm for all measurements, and the LO frequency is greater than the RF frequency. The measured conversion gain, single sideband noise figure, isolation, output TOI, and return loss are shown in Figures 5, 6, 7, 8, and 9 respectively. The conversion gain and SSB noise figure vs. LO drive are shown in Figure 10.

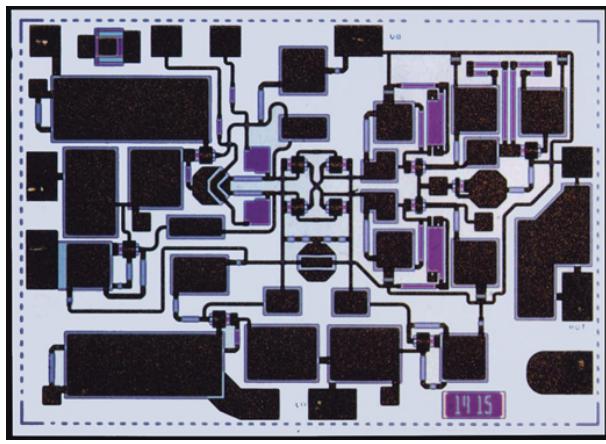


Figure 4. Fabricated Downconverter MMIC.

### Conclusion

Performance of a wideband, pHEMT Gilbert cell downconverter MMIC has been demonstrated. The circuit has 300-8000 MHz bandwidth for RF-LO ports and 185-2085 MHz bandwidth for the IF port. The MMIC is designed for low power +3.0 V operation drawing 17 mA of DC current and requiring a nominal LO drive level of -5 dBm. The circuit is DC blocked, requires no external matching elements, and provides better than 10 dB return loss at all RF ports. At an IF of 185 MHz the conversion gain is 11-15 dB and the SSB noise figure is 9.5-13 dB over an RF-LO bandwidth of 300-8000 MHz. The LO-RF to IF isolations

are better than 30 dB, and the OTOI is typically +5 dBm. This MMIC will provide a high performance, low power option for satellite communication systems.

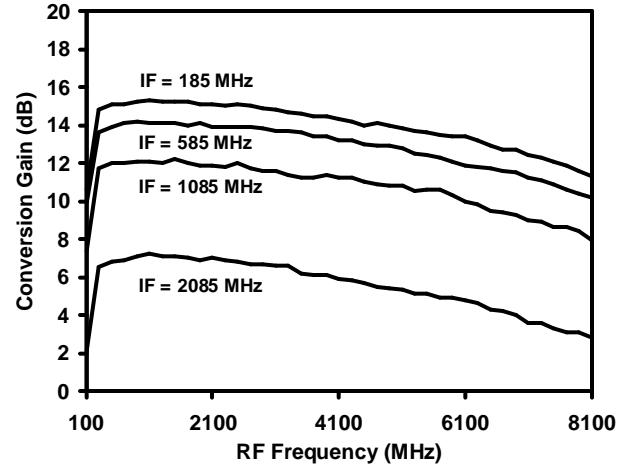


Figure 5. Conversion gain.

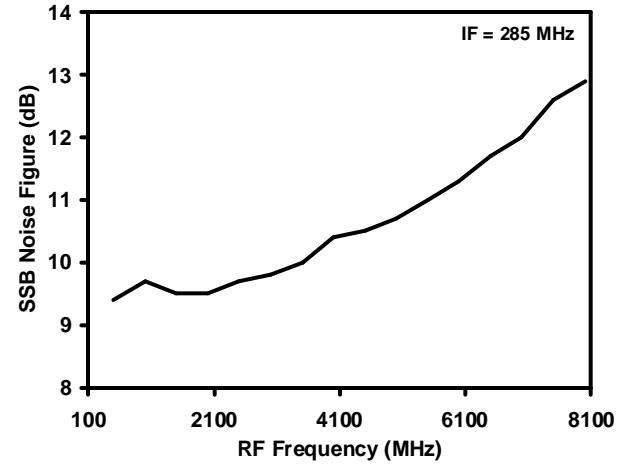


Figure 6. SSB Noise Figure.

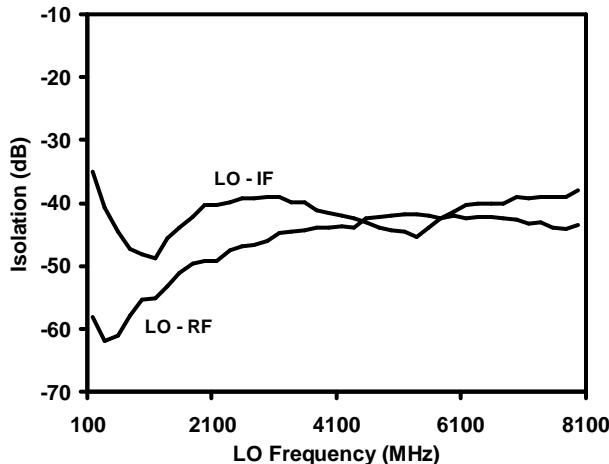


Figure 7. LO Isolation.

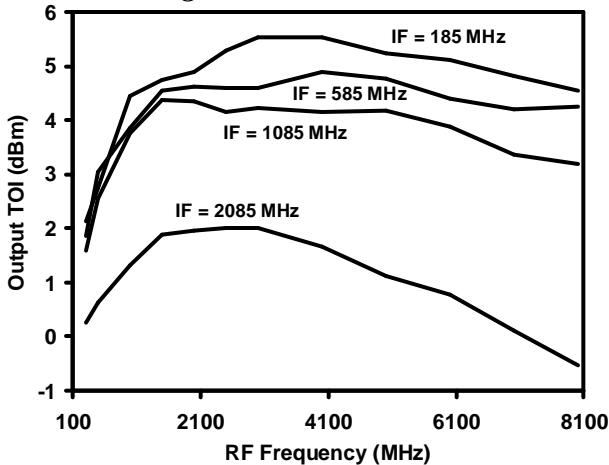


Figure 8. Output TOI.

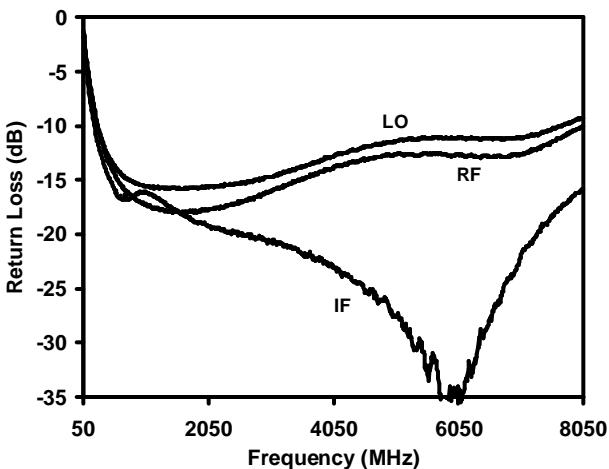


Figure 9. Return Loss.

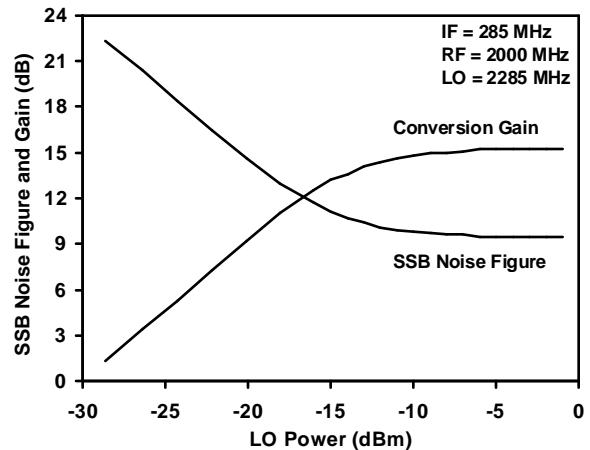


Figure 10. NF and Gain vs. LO Power.

### Acknowledgments

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### References

- [1] Vendelin, G. D., Pavio, A. M., and Rohde, U. L., *Microwave Circuit Design Using Linear and Nonlinear Techniques*, New York: John Wiley & Sons, 1990.
- [2] Maas, S. A., *Microwave Mixers*, Boston: Artech House, 1993.
- [3] Gray, P. R., and Meyer, R. G., *Analysis and Design of Analog Integrated Circuits*, New York: John Wiley & Sons, 1993.